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Amendment and/or Response
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REMARKS

Claims 9-18 are pending in this application. Claims 4-7 are canceled herein.

The applicant respectfully requests the admittance of this amendment, to place the claims in a better condition for allowance or appeal. The claims are rewritten to better conform to U.S. patent practice. The applicant respectfully submits that this amendment adds no new matter, and does not require an additional search.

The Office action rejects claims 4-7 under 35 U.S.C. 102(b) over Walton ("R-CODE A Very Capable Virtual Computer"; PhD Thesis, Harvard University, 1995). The following comments regarding Walton are provided with respect to the rewritten claims.

Claim 9, upon which claims 10-13 depend, claims a method that includes communicating a reference indicator from a first functional module to a second functional module, the reference indicator being indicative of a location of a third functional module in a memory, and executing the third functional module from the second functional module based on the reference indicator.

At the cited text of Walton, Walton teaches a memory management system with automatic garbage collection. Walton uses conventional two-level, or indirect, addressing to provide access to objects in memory: "when an object is copied, the only way to immediately forward all pointers to the object seems to be to make all accesses of the object use indirect addressing through a table location that holds the current address of the object." (Walton, page 31, lines 7-9.) That is, each access to an object will reference a location in a memory map, and as the object is moved or deleted, the new address is placed in the memory map, so that a subsequent access to the memory map for the object will return the new address.

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Walton does not teach that the new address of a functional module/object is communicated from one module to the next, as taught by the applicant. Walton does not teach that the address of a third module is passed from a first module to a second module to facilitate the execution of the third module from the second module, as specifically claimed.

Claim 14, upon which claims 15-16 depend, claims a system that includes a processor and memory that includes at least a first, second, and third module, wherein the first module causes the processor to communicate a reference indicator to the second module, and the second module is configured to cause the processor to execute the third module based on the reference indicator.

As noted above, Walton does not teach that the address of a third module is passed from a first module to a second module to facilitate the execution of the third module from the second module, as specifically claimed.

Claim 17, upon which claim 18 depends, claims a computer program that causes a processor to determine reference indicators corresponding to locations of functional modules, and, upon commencement of execution of each module, causes the processor to communicate a reference indicator to the module, and to execute another module based on the reference indicator that was communicated to the module.

As noted above, Walton does not teach that the addresses of other modules are passed to each module to facilitate the execution of the other modules from each module, as specifically claimed.

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In view of the foregoing, the applicant respectfully requests that the Examiner withdraw the rejections of record, allow all the pending claims, and find the present application to be in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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